Lesson 3 : 8085 Microprocessor Architecture

3.1. Learning Objectives

On completion of this lesson you will be able to :

- recognize the functions of various pins of the 8085 microprocessor.
- list the various internal units that make up 8085 architecture, and explain their functions decoding and executing an instruction.
- draw the block diagram of an 8085 base microcomputer.

3.2. The 8085 MPU

We define the MPU as a device or a group of devices (as a unit) that can communicate with peripherals, provide timing signals, direct data flow, and perform computing tasks as specified by the instructions in memory.

The term Micro Processing Unit (MPU) is similar to the term Central Processing Unit (CPU) used in traditional computers. We define the MPU as a device or a group of devices (as a unit) that can communicate with peripherals, provide timing signals, direct data flow, and perform computing tasks as specified by the instructions in memory. The unit will have the necessary lines for the address bus, the data bus, and the control signals, and would require only a power supply and a crystal (or equivalent frequency - determining components) to be completely functional.

Using this description, the 8085 microprocessor can almost qualify as an MPU, but with the following two limitations.

1. The low-order address bus of the 8085 microprocessor is multiplexed (time shared) with the data bus. The buses need to be demultiplexed.
2. Appropriate control signals need to be generated to interface memory and I/O with the 8085. (Intel has some specialized memory and I/O devices that do not require such control signals).

The 8085 Microprocessor

The 8085 is an 8-bit general purpose microprocessor capable of addressing 64K of memory.

The 8085 is an 8-bit general purpose microprocessor capable of addressing 64K of memory. The device has forty pins, requires a +5 V single power supply, and can operate with a 3-MHz single-phase clock. The 8085 is an enhanced version of predecessor, the 8080A; its instruction set is upward-compatible with that of the 8080A, meaning that the 8085 instruction set includes all the 8080A instructions plus some additional ones. Programs written for the 8080A will be executed by the 8085, but the 8085 and the 8080A are not pin compatible.

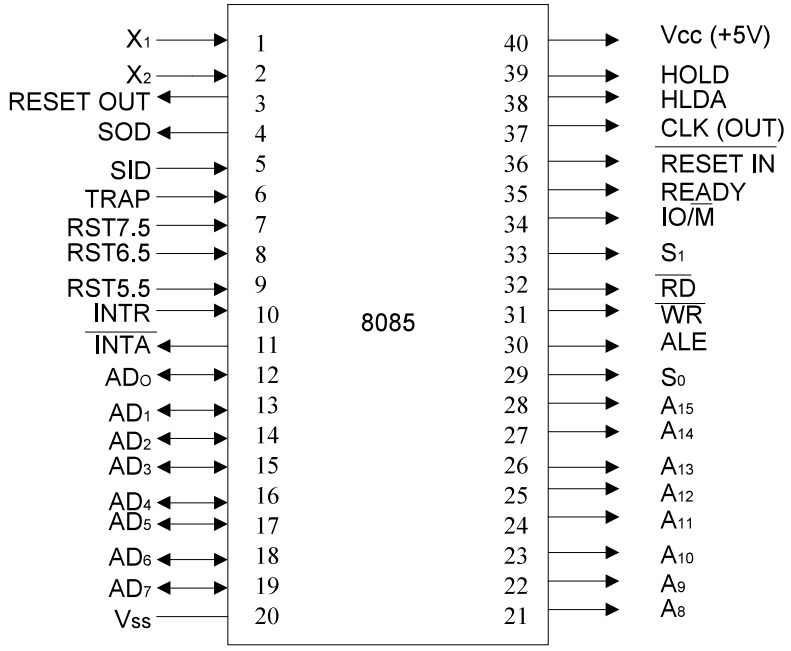

Fig. 8.1 : 8085 microprocessor signals and pin assignments.

Multiplexed Address / Data Bus

Multiplexed address / data bus.

The signal lines AD_7 to AD_0 are bidirectional, they serve a dual purpose. They are used as the low-order address bus as well as the data bus. In executing an instruction, during the earlier part of the cycle, these lines are used as the low-order address bus. During the later art of the cycle, these lines are used as the data bus. (This is also known as multiplexing the bus). However, the low-order address bus can be separated from these signals by using a latch.

Control and Status Signals

Control and status signals.

This group of signals includes two control signals (RD and WR), three status signals (IO/M, S_1 and S_0) to identify the nature of the operation, and one special signal (ALE) to indicate the beginning of the operation. These signals are as follows :

- ALU - Address Latch Enable : This is a positive going pulse generated every time the 8085, begins an operation (machine cycle); it indicates that the bits on AD_7 - AD_0 are address bits. This signal is used primarily to latch the low-order address from the multiplexed bus and generate a separate set of eight address lines, A_7 to A_0.

- RD - Read : This is a Read control signal (active low). This signal indicates that the selected I/O or memory device is to be read and data are available on the data bus.
- WR - Write : This is a Write control signal (active low). This signal indicates that the data on the bus are to be written into a selected memory or I/O location.
- IO/M : This is a status signal to differentiate between I/O and memory operations. When it is high, it indicates and I/O Operation; when it is low, it indicates a memory operation. This signal is combined with RD (Read) and WR (Write) to generate I/O and memory control signals.
- S_1 and S_0 : There status signals, similar to IO/M, can identify various operations; but they are rarely used in small systems.

Power Supply and Clock Frequency

Power supply and clock frequency.

The power supply and frequency signals are as follows :

- V_{CC} : + 5 volt power supply.
- V_{SS} : Ground Reference.
- X_1, X_2 : A crystal (or RC, LC network) is connected at these two pins. The frequency is internally divided by two; therefore, to operate a system at 3 MHz, the crystal should have frequency of 6 MHz.
- CLK (OUT) - Clock Output : This signal can be used as the system clock for other devices.

Interrupts and Externally Initiated Operations

Interrupts and Externally Initiated Operations.

The 8085 has five interrupt signals that can be used to interrupt a program execution. Once of the signals, INTR (Interrupt Request), is identical to the 8080A microprocessor interrupt signal (INT); the others are enhancements to the 8080A. The microprocessor acknowledges an interrupt by the INTA (Interrupt Acknowledge) signal.

In addition to the interrupts, three pins - RESET, HOLD, and READY - accept the externally initiated signals as inputs. To respond to the HOLD request, it has one signal called HLDA (Hold Acknowledge). The RESET is again described below.

- ***RESET IN :*** When the signal on this pin goes low, the program counter is set to zero, the buses are tri-stated, and the MPU is reset.
- ***RESET OUT :*** This signal indicates that the MPU is being reset. The signal can be used to reset other devices.

Serial I/O Ports

The 8085 has two signals to implement the serial transmission : SID (Serial Input Data) and SOD (Serial Output Data).

3.3. Exercise

3.3.1. Questions for short answers

a) What are the functions of 8085 microprocessor?
b) What are control and status signals?

3.3.2. Analytical question

a) List the internal units of 8085 architecture and explain their function.